Software Defined Radio (SDR)

Overview

This SDR system is a flexible, high-performance platform built around the AD9361 wideband RF transceiver and Xilinx Zynq XC7Z100 FPGA. Supporting a frequency range from 200 kHz to 6 GHz, it enables dual-channel Tx/Rx with real-time signal processing and control. Its adaptable architecture allows customization of the RF front-end and clock configuration, making it ideal for diverse and evolving communication applications.

Key Features

1. Integrated RF Transceiver

- Wideband coverage: 70 MHz to 6 GHz.
- Zero IF dual-channel transceiver with 2x2 MIMO support.

2. Zynq-7100 SoC

- High-performance programmable logic for flexible signal processing.
- Dual-core ARM Cortex-A9 CPU operating at 800 MHz with 256 MB DDR3 RAM.

3. Dual-Channel Tx and Rx

- Simultaneous Tx and Rx operations.
- Wide tunable frequency range: 70 MHz to 6 GHz.
- Up to 56 MHz instantaneous bandwidth.

3. Comprehensive Interface Options

- Micro-USB ports (serial console, JTAG).
- Ethernet (1 RJ45 port with 1 GbE).
- FMC connector for modular expansion.
- GPIO header for general-purpose I/O.

5. Software

- Compatible with LabVIEW, OpenEmbedded Linux, Vivado SDK, GNU Radio, RFNoC, and C/C++.

6. Flexible Boot Options

- SD Card, JTAG, EMMC Flash, and QSPI Flash support.

7. Enhanced Application Compatibility

- Interfaces with bias tees and band-pass filters for specialized applications.

Technical Specifications

1. RF Characteristics

- **Frequency Range (Tx & Rx):** 70 MHz to 6 GHz
- **Architecture:** 2x2 Zero IF Transceiver
- **Channel Bandwidth:** 200 kHz to 56 MHz (tunable)
- **Receiver Gain:** 0 to 74 dB (1 dB step, frequency dependent)
- **Transmit Power Control Range:** 90 dB (0.25 dB resolution)

2. Digital Features

- **Memory:** DDR3, 2048 Mb
- **Interfaces:** USB-UART, Ethernet, FMC, GPIO Header
- **Gain Step:** 1 dB
- **Gain Range:** 0 to 73 dB

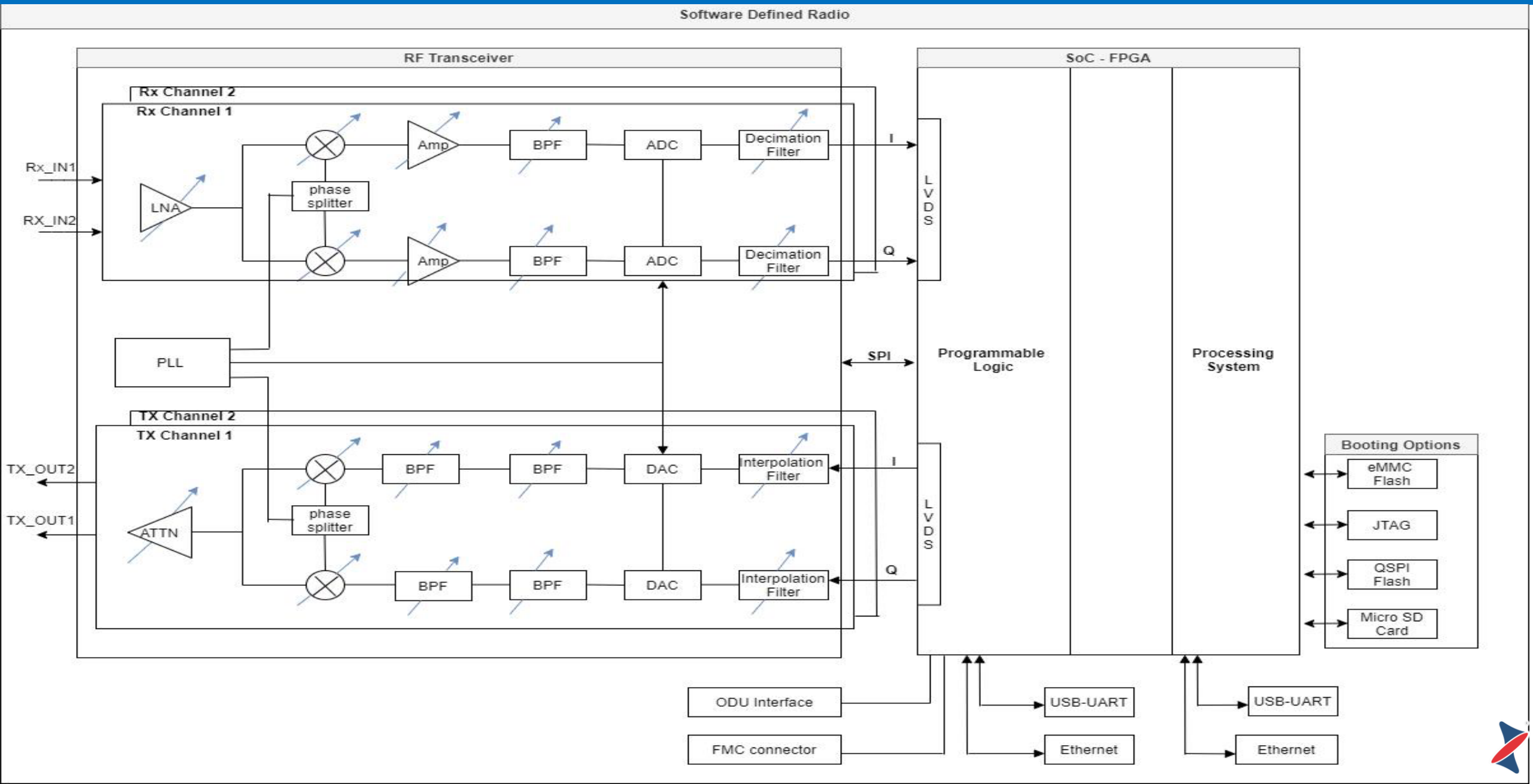
3. Other RF Features

- **LO Frequency Step:** >2.4 Hz (for 40 MHz reference clock)
- **DAC Resolution:** 12 bits
- **ADC Resolution:** 12 bits
- **Internal Reference Clock:** 40 MHz, 0.5 PPM stability
- **Reference Clock Options:** Internal (TCXO) and External (10 MHz)

4. Power Supply

- **Input Voltage:** 28.0 V DC
- **Current:** 1 A

System Architecture



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Thank You !

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